Asvoria Kuan Soo Huey

Email: asvoria@live.com
Phone: +6016-4713138
Web: https://asvoria.github.io/MyCV/

Engineer with strong technical knowledge and hands on experience. Over 12 years working in the electronics industry. Started her own electronic product business, build up a product. Electronics hardware from architecture, schematic, simulation, PCB floor-planning, routing, BOM, assembly, testing, FA, to final documentation of her invention. Also profess in IC design, from RTL to schematics, to mask/layout design of 14nm (or less) technology. Also an expert in C/C++/C# programming. She believes all computer languages are the same! Regardless of java python solidity or any new languages that a computer may understand: codes.

Current Projects

SmartLoan

https://smartloan.github.io/smartloan-page/
A DeFi Solution to Student Debt Crisis!

SmartLoan is a Proof of Concept P2P loan DeFi prototype for the digital future which attempt to solve student debt crisis. It attempt to bridge between permissionless and permissioned chains, providing a low risk, secured and collateral-free lending that benefits both borrowers and lenders. The design of negative interest rates calculated based on monthly repayment principal, and positive interest rates based on the debtor's net income.

Enhance utilization and investment sentiment on Decentralized Financial (DeFi) product through government regulated Decentralized Identifiers Documents(DID)

This is an interdisciplinary research that covers computer science, banking and finance topics. It focus mainly on the network trusted identity authentication technology implementation on decentralized financial and banking system to achieve new findings on users sentiment, attempt to answer the following questions…

1. To what extend the government regulation of DeFi products help to bring up user awareness on cybercrime, and thus, reducing DeFi related scams?
2. How the bridging between government regulated permissioned network and permissionless blockchain can improve the adoptability of a DeFi product?
3. Does government regulation lead to greater success in DeFi utilization and investment?

Previous Projects

BOLT - Low Frequency Global Lightning Location System

2018

Project lead by Prof Zen Kawasaki for Rairan (Singapore) Pte Ltd

Additive Manufacturing Technology - Will It Disrupt the Traditional Patent Legal System? A Study Based on TRIPs, PCT and National Patent Law of Malaysia and Singapore, compared to EU and US law.

2015

A thesis for LLM. Master of Law (Intellectual Property)

Haswell (Intel)

2009 - 2012

Design of circuitry schematics and mask layout for register file fubs in desktop microprocessor. Also involved in multiple of repeater fub works.

Westmere (Intel)

2008 - 2009

Design of mask layout for analogue fubs in desktop microprocessor.

Design and Prototyping of Wireless Machine Management System (IOT/SCADA)

2008

Final Year Project for Bachelor's Degree of Engineering (Microelectronics)

Technical Mentor of Commonwealth Secondary School (SG) for 19th Youth Science Conference 2013 (SG)

2013

Volunteer as technical mentor to guide normal secondary school students to accomplish science fair projects and compete in an event for gifted students. Technical information provided to the students to design and build a Tesla coil, perform tests and measurement generated by it. The purpose of this project is to bring in normal secondary students who are interested in scientific research to complete and share their findings.

Software Development of Library Management System

2013

For Skudai (Johor) Chinese Methodist Church. Set up the whole library management system from scratch. The software is programmed by C#, including utilities which allows librarian to directly retrieve all books' information from Google Books database. The software involves parsing of JSON to XML to strings which will be processed by C# instructions. The software interface is easy to use & bilingual (Mandarin & English).

Employment History

Continental Electronics (Singapore) Pte Ltd

https://www.continental.sg/

Senior Embedded System Engineer

Dec 2019 - Present

Development and prototyping of various electronics products. Sky is the limits!

Alam Pelangi Envirotech (Malaysia)

Founder Engineer

Dec 2018 - Dec 2019

Development and prototyping of IOT product, bridging the analogue world to digital computing. Implementing high precision, super speed analogue-to-digital module. Negotiate with potential customers, vendors, and managing engineering, marketing and sales team. Response and bid on call-for-tender projects. Seeking and pitching for investors to help accelerate the completion of the project.

Southern University College (Johor, Malaysia)

Lecturer

Sep 2017 – Dec 2018

Covered various engineering topics such as Electronics Instrumentation, VLSI system Design, Digital Signal Processing, Signal and Systems, C/C++/C# Programming and Higher Engineering Mathematics. Successfully guided Diploma Students on their final year projects which encompass various engineering problems.

Usains Infotech (Malaysia) Sdn Bhd (Infinec)

Senior Component Design Engineer

Dec 2016 – July 2017

Successfully completed the designated CBB layout under a contract with our contract client: Intel Microelectronics. Helped the DDR/MIG MD team during the critical transition period from 14nm technology to 10nm technology. Design integrated circuit schematics (ADT DDR) to pass FEV (Formal Equivalence Verification) Tape-in schematics to layout. Design and floorplan digital and analogue layout using Genesys (CAD tool) to meet DRC (Design Rule Check), and RV (Reliability Verification) to tape-in for production.

Hitachi Critical Facilities Protection (Singapore) Pte Ltd

Research Engineer

Jul 2012 – Sep 2015

Leads the R&D team to design new product from concept to micro-production of golden sample. The team had successfully improved the performance of HCFP's core surge protection device and greatly reduce the production costs by re-design the PCB, components and careful selection of new components. She was part of the pioneer R&D

team member who successfully set up a high voltage test lab for HCFP. She build up a 10kV 5kA surge generator to perform tests on new products.

Introduce product concept & solution. Design circuitry, simulation models, build schematics, footprints library, component placement, PCB layout routing, BOM, marketing prototype building, functional prototype building and testing, final production golden sample preparation.

- Design art stages which met DFM, going through TRLA (Technology Readiness Level Assessment) & MRLA (Manufacturing Readiness Level Assessment)
- Working together with procurement to source & negotiates for BOM purchases.
- Plan & perform tests for new products for IEC/UL/JIS standard tests.
- Documentation on product EC self certification.
- Working with marketing to perform public demonstration, expo, shows, & business partner presentation on new products.
- Roadmap & budget planning on new product design.
- Prior art search & evaluating product patentability. Document preparation & log booking for R&D process.
- Develop test methods/technique, integrate and validate test program for surge protection devices and varistor components.
- Customer's site survey to collect realistic data, identify problems and propose new design improvement.
- Meeting with customer to analyse their needs & provide technical support to sales account manager for preparation of quotation for the customers.
- Responsible to set up high voltage test lab. Building of 10kV 5kA surge generator to perform tests on new products.

Intel Microelectronics (Malaysia) Sdn Bhd

Component Design Engineer

Jun 2008 – Jun 2012

Successfully completed the designated fub layout for Westmere and Haswell projects on schedule. At the same time, she provided support for her colleagues on their fubs. During the 2nd year of her employment, she expanded her career by taking up schematic design for RF (Register Files) fubs.

Design integrated circuit schematics (Register Files) to pass FEV (Formal Equivalence Verification), converge timing, power, noise and quality requirements internally and externally to section.Re-design and implement new schematic topology to meet timing and power requirement.Tape-in schematics to layout. Design digital and analogue layout using Genesys (CAD tool) to meet DRC (Design Rule Check), and RV (Reliability Verification) to tape-in for production. Chartered 28nm layout design to meet DRC & production rules. Digital core RF (Register Files) circuit design from RTL to schematics.

- 4 years Digital Integrated Circuit mask design experience.
- 1+ years Analogue Integrated Circuit mask design experience.
- 1+ years Digital Integrated Circuit design experience.

Education Background

Southern University College, Johor, Malaysia
PhD by Research (Blockchain, DeFi, DID)
Jun 2021 – present

University of Turin (UNITO), Italy
LLM. Master of Law (Intellectual Property)
Jun 2014 – Feb 2015

University Malaysia Perlis (UNIMAP), Malaysia
Bachelor's Degree of Engineering (Microelectronics)
Jun 2004 – Aug 2008

EdX Certificates

- LFS172x - Introduction to Hyperledger Sovereign Identity Blockchain Solutions - Indy, Aries & Ursa
- BerkeleyX - CS198.2x Blockchain Technology
- HarvardX - GSE2x, Leaders of Learning

Skills

Programming - expert in C/C++/C# but flexible on all other programming languages. An advocate for the concept of teaching C as “Mother of all programming languages”. Profess both firmware and software programming.

Electronics circuit design (both digital and analogue circuits), from schematic to PCBA.

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